

REGISTRATION FORM

Name :

IEEE Membership Number
(if applicable) :

Name of the Institution :

Contact address :

Email:

Tel / Cell No :

Details of
Demand Draft

DD No :
Drawee Bank :

Note: The Bank DD shall be drawn in favor of
IEEE Madras section, payable at Chennai.

I certify that I have taught one or more courses on
VLSI.

Signature of the Applicant

Signature of the Head of the Institution

**Complete Registration form along
with demand draft to be sent to**

IEEE MADRA SECTION
Room No 3, ISTE Professional Centre,
Gandhi Mandapan Road, Chennai 600 025

Contact Details for Course

Dr. (Mrs). C. Kezi Selva Vijila
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Electronics and Communication
Engineering
Karunya University
Coimbatore-641 114

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Email: vijila@karunya.edu

**IEEE MADRAS
SECTION**



Course Title

**FPGA BASED SYSTEM DESIGN USING EDA
TOOLS**

Date:
11-12th Sep 2009

Venue:
**Department of
Electronics and Communication Engineering
Karunya School of Electrical Sciences
KARUNYA UNIVERSITY
Coimbatore – 641 114**

**Contact Address
IEEE MADRA SECTION**

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About the IEEE

The Institute of Electrical and Electronics Engineers Inc.(IEEE), a nonprofit organization, is the world's leading professional association for the advancement of technology.

Through its global membership, the IEEE is a leading authority on areas ranging from aerospace systems, computers and telecommunication to biomedical engineering, electric power and consumer electronics among others. The IEEE has more than 365,000 members, including 68,000 students, in over 150 countries. It publishes 128 transactions, journals and magazines and organizes more than 300 conferences worldwide each year.

To foster an interest in the engineering profession, the IEEE also serves student members in colleges and universities around the world.

IEEE Madras Section came into existence in 1978 and has crossed its silver jubilee year. It is organizing Technical Meets, Conferences and Seminars of highest standard for the benefit of its members. The section today has the highest number of student branches among the section in the world. The section is concerned about the welfare of the students in this part of country and wants to improve the teaching-learning process in the Engineering colleges and Universities. With this in mind, the section is organizing **Faculty Development Programme (FDP)** for the teaching faculty members of Engineering Colleges and Universities in Tamil Nadu

Faculty Development Programme:

The whole world is at the dawn of the greatest revolution of the mankind nanotechnology. The influence of nanotechnology is on all branches of Engineering and science. VLSI Design (a branch of nanotechnology) is

experiencing tremendous growth due to advances in technology and scaling in size of devices. As designers have to pack more devices in a VLSI chip, the process of generating layouts is also becoming increasingly complex. CAD tools have to deliver effective solutions for vastly scaled up problems and in the presence of very stringent constraints. A designer must understand the problems associated with the design as well as the workings of CAD tools to arrive at early design closure. This workshop is designed for introducing the tool to understand the MOS characteristics with user interface. It has different modules for transistor level layouts, mixed signal simulation and memory simulator.

Schedule:

The Course on "FPGA based System design using EDA tools" is proposed to be held on Sep 11th and 12th, 2009. The programme will be for two days with 4 sessions, each of 3 hours duration.

Participants:

Those people who wish to pursue research and / or career in the field of VLSI CAD must take this course. VLSI engineers who wish to become better designers by clearly understanding the complexities of design, tools, and problems will benefit from this course.

Course Fee:

There is no course fee for IEEE members and for non-members the course fee is Rs.1000/-. Non members will be refunded the course fee if they become member within one year, The number of seats is limited and the participants will be chosen on a first-come-first-served basis provided they satisfy the criterion of having taught a course in related area. The fee includes course material and lunch. Accommodation and transport will be the responsibility of the participants.

Course Title

FPGA based system design using EDA tools

Course Content:

CMOS VLSI Design flow & HDL Based Logic

- VLSI Design flow
- MOS realization of Digital circuit
- HDL language
 - ✓ VHDL
 - ✓ Verilog

HDL & Tanner Lab

- Pre-layout simulation using XILINX tool
- FPGA implementation of Digital logic-Spartan FPGA
- Power analysis using Tanner tool

Mentor graphics Lab

- Semi custom design
- Layout design
- Full custom design

HDL Lab using ALTEA Tool

- Pre-layout simulation
- Area analysis
- Delay analysis
- Power analysis

Course Instructors

Mr.R. Dhamodaran, Director/CISCO

Mr. Jebin Vijay, CMR Automation, Bangalore

Dr. S. Srinivasan, IITM

Dr. P.T. Vanathi, PSG Tech

Mr. P. Karthigaikumar, Karunya

Mr.S. Nireekshan Kumar, Karunya